RFL Electronics Inc.

INSTRUCTION DATA

66A DEC Decoder Controller
and
66A DEC EXP Decoder Expander
HD-44963-JMC-1

PREFATORY NOTE

This data sheet describes Model 66A DEC Decoders and Model 66A DEC EXP Expanders assembled on printed-circuit boards which bear the identification HD-44963-JMC-1 (or higher suffix digits) at the approximate top-center area of the component side of the circuit board. These data do not pertain to circuit modules assembled on boards bearing the identification HD-44963-JMC, and those holding such boards should request RFL for a different data sheet, which is available. A statement giving the number appearing on the board of interest will be helpful in filling such requests.

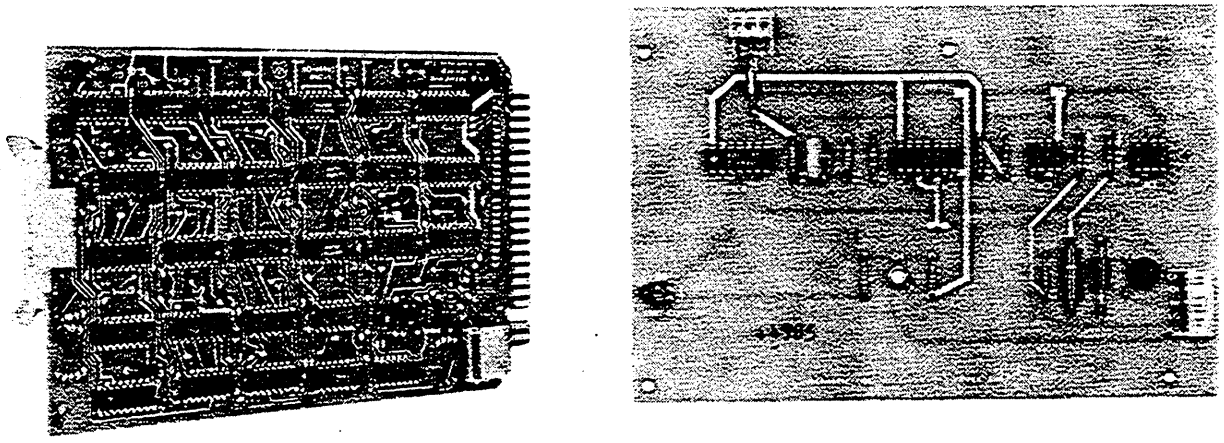


Figure 1. Model 66A DEC Decoder Controller. Plug-on metallic-line receiver is shown at right.

DESCRIPTION

The Model 66A DEC Decoder Controller is one of the logic modules in the RFL Series 6644/6850 Time-Division Multiplex System. As a receiving device, it complements the Model 66A ENC Encoder Controller used at the sending end of a TDMS system. The 66A DEC receives encoded serial data and develops a parallel-data output corresponding to the data-input status of the corresponding 66A ENC. A block diagram of the circuits of the decoder is shown as Figure 2.

The Model 66A DEC will handle up to sixteen data points. The system may be expanded indefinitely, in increments of sixteen data points, for each Model 66A DEC EXP-N Decoder Expander added in series with the system.

The decoder is designed to be used with the RFL Model 68B FSRX receiver as an interface with the communication facility. It can also be used with many other voice-frequency, carrier-telegraph receivers. An optional plug-on metallic-line receiver is also available on special order to interface with dc lines. Change of state can be communicated and recognized by turning off the carrier of the 68B FSTX at the encoder end.

A RELEASE DATA lamp pulses each time valid data are loaded into the output registers. A SCAN FAIL lamp gives a delayed, continuous indication of failure of the decoder to release valid data.

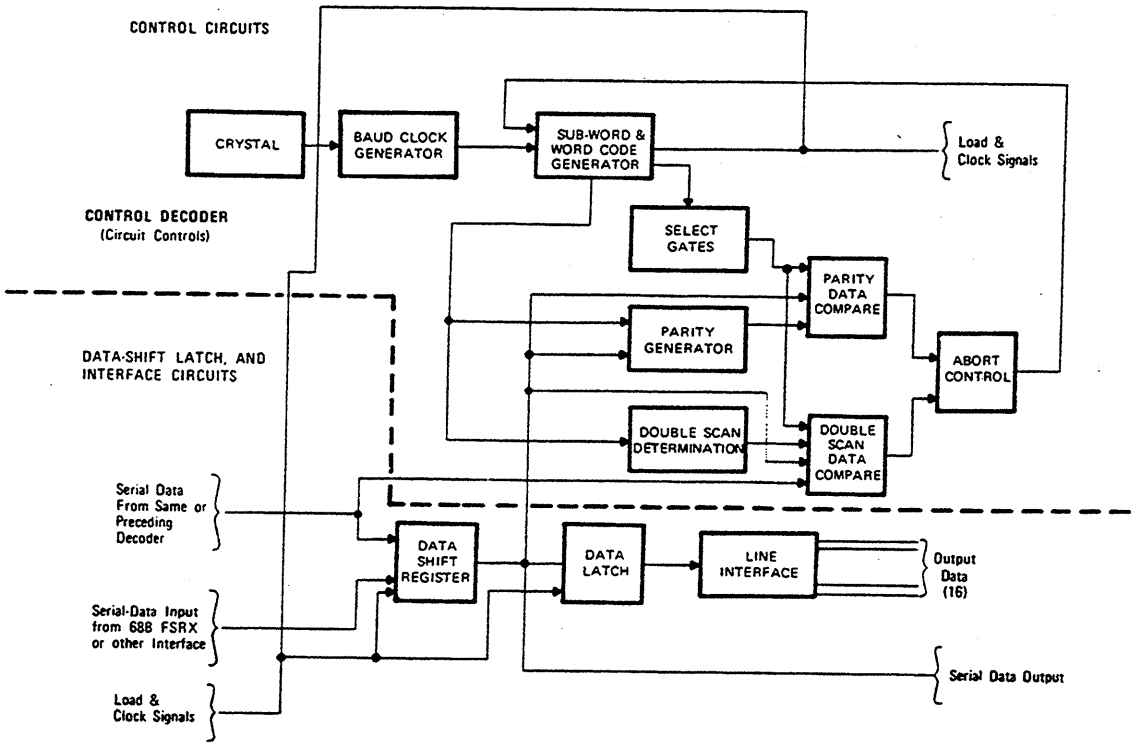


Figure 2. Block diagram of circuits of Models 66A DEC and 66A DEC EXP.

SPECIFICATIONS

Number of Data Bits: The Model 66A DEC Decoder Controller controls the level of 16 data points. The system can be expanded to 32, 48, and 64 bits (double scan) or in multiples of 16 bits to a total of 144 bits (single scan) with the addition of Model 66A DEC EXP-1 Decoder Expanders.

Input: The input circuits are CMOS-compatible, and they will respond to output signals from RFL FSK receivers such as the Models 68B FSRX and 68R, and the metallic-line driver which is an optional plug-on accessory to the Model 66A DEC.

Data Rate: 60 baud is standard. Rates of 120, 240, and 480 are available on the same module by changing jumpers. Rates from 35 to 1600 are available on special order.

Code: Each message word begins with a header and contains two parity and sixteen data bits. Doublescan is standard, singlescan is optional. Code format is detailed in the text.

Output Circuits: Open-collector outputs to common will sink a minimum of 120 mA, and will withstand 50 Vdc simultaneously at all outputs. Optional output-relay mountings are available for use with these units, and optional pull-up resistors may be included.

Time for Scan: At 60 baud with doublescan, a scan requires 1.1 seconds (66 bits). With singlescan the period is 0.57 second (34 bits).

Security: Parity and doublescan are standard. Single-scan is optional. A supervisory lamp and an open-collector closure to common indicate failure of scan.

Indicators: Supervisory lamps indicate data release and failure of scan.

Power Turn-On: During power turn-on, outputs are set to the non-conducting state.

Output-Register Reset On Scan Failure: An optional feature allows the output to go to the non-conducting state upon failure of scan.

Operating Ambient-Temperature Range: −30 to 70°C.

Power Requirements: 11 to 13 Vdc, 30 mAdc, with all outputs open.

Size: Each card occupies two standard one-half-inch module spaces in an RFL Model 68 Chassis.

Metallic-Line Receiver, Option HB-44985:

Maximum Usable Baud Rate: 600 baud.

Maximum Total Line Resistance: 400 ohms.

Power Required: 11 to 13 Vdc, 10 mAdc maximum.

ORDERING INFORMATION

A baud rate of 60 and doublescan are standard. Single-scan and other speeds are available on special order, in which case the desired operating baud rate must be specified from Table 1, and the desired message format from Table 2 should be stated. Specific model designations for standard modules are given in the accompanying table.

If the metallic-line receiver, available on special order only, is required, the need should be stated.

A connector wiring assembly is available for easy field wiring of the module into a properly equipped RFL Model 68 Chassis. When this connector assembly is used, the number of data points available is eight. The external chassis wiring is shown in Figure 3.

SERIES 66 TDMS Model 66A Decoders	HB-44960 Decoder	HB-44965 Decoder Expander	HB-45440 Resistor Networks RZ1, 2
66A DEC	•		
66A DEC EXP-1		•	
66A DEC-1	•		•
66A DEC-EXP-2		•	•
Applicable Connector Assy. HB-90844			

Connections shown below apply when the specified connector assembly is used. When chassis are completely wired by RFL, a connection diagram is furnished.

Note: Only 8 outputs are available when the connector assembly is used.

The uncircled number shown at the right indicates the data position in the serial pulse code, and corresponds to the respective input and output points of encoders and decoders.

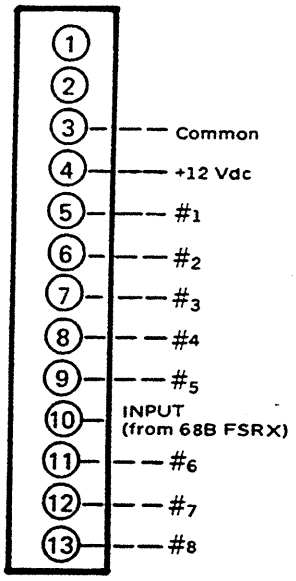


Figure 3. Terminal assignments for connector-wiring assembly.

CODE FORMAT

Each word is made from four subwords, and each word is comprised of the serial data generated by one encoder card.

The first subword is an unique ten-bit stream of ten logic lows which synchronize the system. Each of the remaining three subwords carries data bits, while the fourth and final subword also carries two parity bits which indicate the two least-significant bits of the binary sum of all high data bits for the entire word.

Each message may contain one or more words. They use the same format as the first word except that the first subword contains all logic highs, is not unique to the system, and so can not be confused as a header signifying the beginning of a message.

The message used for doublescan consists of word sequences transmitted twice. The word header of the second scan, however, consists of highs, and the subwords will be inverted on the second transmission.

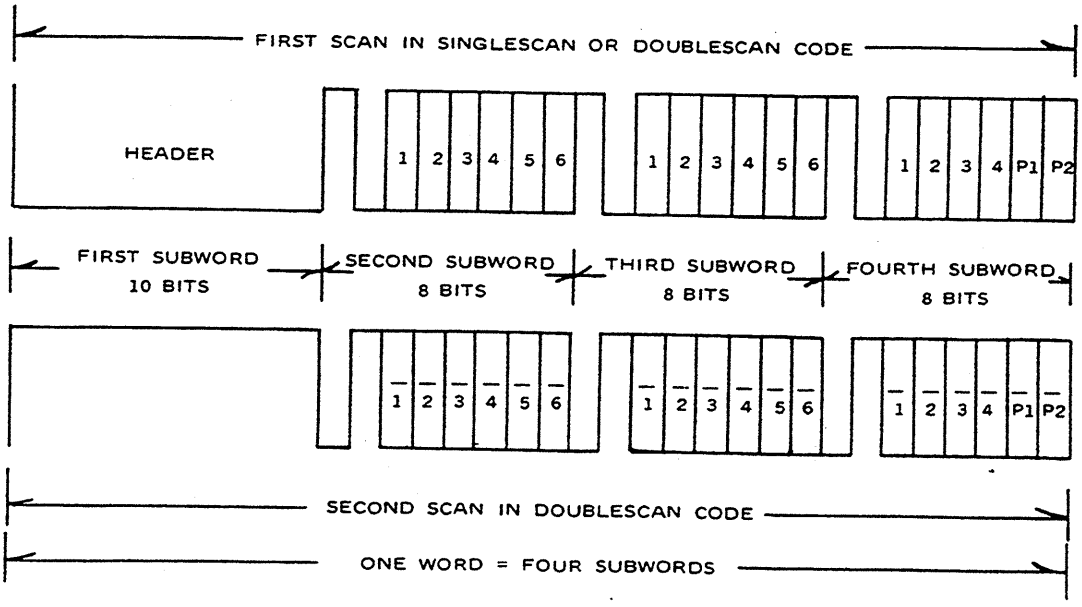


Figure 4. Code format used for Model 66A DEC.

PROGRAMMING AND CONNECTIONS

All semiconductors, and especially smaller ones such as small-signal transistors, linear and digital integrated circuits, and microprocessors, are vulnerable to the possibility of damage from static charges. Procedures for minimizing this possibility are outlined in RFL Document 12175A.

All unused input terminals should be returned to +V or to circuit common.

Circuit

As indicated in the block diagram, the circuit card is divided into two sections: (a) a circuit-control section, and (b) a data-shift, latch, and interface section. The Model 66A DEC uses both sections. The Model 66A DEC EXP requires only the data-shift, latch, and interface section.

Baud Rate

The baud rate of the decoder is set at the factory. It is determined by selecting a quartz crystal of appropriate frequency and by setting jumpers, as shown in Table 1.

TABLE 1

BAUD-RATE PROGRAMMING & CRYSTAL OPTIONS

Baud Rate	Suffix to Crystal's P/N HB-37440-(**)	Crystal Freq. MHz	BAUD Jumper
1600	-51	3.2768	F
1280	-99	2.6214	E
1200	-97	2.4576	F
1120	-98	2.2938	F
960	-53	3.9321	E
800	-51	3.2768	E
640	-99	2.6214	E
600	-97	2.4576	E
560	-98	2.2938	E
480	-53	3.9321	D
400	-51	3.2768	D
320	-99	2.6214	D
300	-97	2.4576	D
280	-98	2.2938	D
240	-53	3.9321	C
200	-51	3.2768	C
160	-99	2.6214	C
150	-97	2.4576	C
140	-98	2.2938	C
120	-53	3.9321	B
100	-51	3.2768	B
80	-99	2.6214	B
75	-97	2.4576	B
70	-96	2.2938	B
60	-53	3.9321	A*
50	-51	3.2768	A
40	-99	2.6214	A
35	-98	2.2938	A

*Denotes standard model.

Message Length

Each message contains one or more words. Each word contains 16 data bits, and associated control bits. Table 2 illustrates the jumper-selection procedure used to establish different message lengths. A separate Model 66A DEC EXP is required for each additional group of 16 data points.

TABLE 2

MESSAGE-LENGTH PROGRAMMING

Message Length	SCAN	SCAN Jumper	WORD Jumper
1	Single	N	1
1	Double	1	2*
2	Single	N	2
2	Double	2	4
3	Single	N	3
3	Double	3	6
4	Single	N	4
4	Double	4	8
5	Single	N	5
6	Single	N	6
7	Single	N	7
8	Single	N	8
9	Single	N	9

Supervisory Lamps

The SCAN FAIL indicator lamp requires scan failure to persist for approximately 5 to 15 seconds before operating. Cancellation of the indication requires the same delay time.

The RELEASE-DATA indicator will give a continuous dim glow at high baud rates, and it will pulse at the expected message rate when lower baud rates are used.

Intraboard and Interboard Wiring

The intraboard wiring of a one-word-message decoder is treated in the same manner as is the wiring of a multiword message-decoder system. For message-length expansion, Model 66A DEC EXP Decoder Expander cards are connected in series with a Model 66A DEC Control Decoder card. The control decoder card must be positioned to interface with the initial serial-data output from the receiving device.

For series-connected decoders, each MULTIWORD DATA OUTPUT, Terminal D, is connected to the succeeding decoder's EX DATA IN, Terminal L. The control decoder's DATA IN, Terminal W, will be connected to the CMOS-compatible output of the line-interface device. If the Metallic-Line Receiver, Option HB-44985, is used, the HIGH and LOW INPUTS, Terminals 21 and 22, are connected to compatible lines, and DATA IN remains unconnected.

For doublescan applications, the DOUBLESCAN DATA OUTPUT, Terminal E, of the final, or only, decoder card in the system is connected to the control decoder's DOUBLESCAN DATA INPUT, Terminal M.

The serially connected decoder cards must have their INITIALIZATION inputs, Terminal S, interconnected. Similarly, SHIFT CLOCK, Terminal F; LOAD CMND, Terminal C; and REG RESET, Terminal 19 are respectively interconnected among cards.

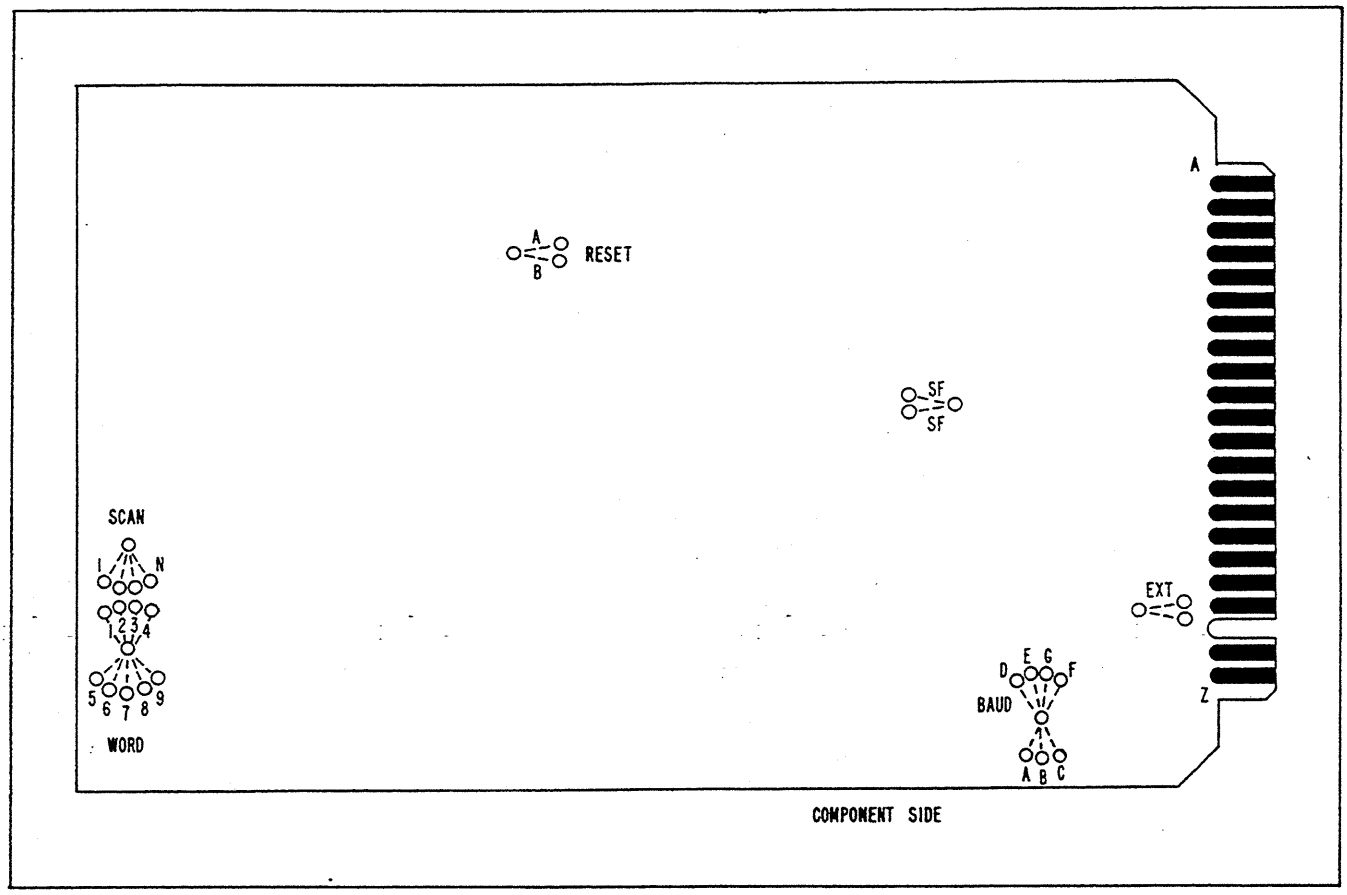


Figure 5. Location of jumpers, Model 66A DEC and Model 66A DEC EXP.

Output registers may be reset manually by connecting REG RESET, Terminal 19, to signal common through a normally open contact.

A continuous high must be maintained on the $\overline{CF}$ line to enable the decoder. This feature serves as a carrier-fail-safe guard.

Data Outputs

The data outputs are open-collector drivers. Figure 6 illustrates the output connections. Individual open-collector outputs can sink 400 mA, but the total current in each package, in elements QZ1, QZ2, and QZ3, must not exceed 700 mA.

For series-connected decoder cards, **the control decoder card's output data corresponds to the initial encoder extender card's input data. Correspondingly, the control encoder card's data corresponds to the final decoder extender card's output data.**

If optional pull-up resistors are included, Jumper +V will be used to pull up the resistor network to the +V of the card, or Jumper EXT can be used to connect the network through DATA EXTERNAL PULL–UP SOURCE, Terminal V, to an external source.

Output-Register Reset

If the output register must be reset during scan fail, Jumper RESET A, Figure 5, should be used. Output-register reset will occur approximately five to fifteen seconds after continuous failure to decode the data properly. For non-automatic register reset, use Jumper RESET B. External register reset uses Jumper RESET B, and is accomplished with a contact closure to common of Terminal 19, REGISTER RESET.

$\overline{\text{DELAY ERROR SCAN}}$ open-collector-output Terminal J generates an output approximately five to fifteen seconds after a continuous failure to decode the data properly, when Jumper $\overline{SF}$ is employed. If Jumper SF is used, the output DEL ERROR SCAN, Terminal J, goes into a high-impedance state after a scan failure.

The $\overline{\text{UPDATE}}$ open-collector output, Terminal K, develops an output when the output-data latches are being updated. The output latches are updated on the initial high-to-low transition of this output.

Interface with Tone Receiver

When the decoder is used with an RFL Model 68R 2F/3F Receiver, or with a Model 68A TX/RX Transceiver, the receiver should be set so that its signal-output terminal goes to a logic high in the event of carrier failure.

When carrier detection is used with the Model 68A TX/RX, a Type 1N914B diode must be inserted at Jumper Position 8C-8D. The anode on the 8C side provides for high CD output signal when carrier is present.

Code Security

It is recommended that doublescan be used in this system. A fifty-percent bias distortion may cause erroneous data in singlescan systems.

Relay-Coil Diode Protection

DIODE, Terminal H of both the decoder controller and the decoder extender cards, is the common output of the diodes used for protection against inductive-voltage spikes caused by opening the coil of a relay. Terminal H should be tied to the positive side of the source used to power the relay's coil. Note that:

(a) The source used to power the relay must be equal to or higher in voltage than the supply used for the circuit card, and

(b) When Terminal H is used, the power source must be the same for all components connected to the individual decoder cards.

Error Scan Failure

Jumper SF will cause $\overline{\text{DELAY ERROR SCAN}}$ signal, Terminal J, to be a delayed low on conduction-to-ground state after a scan fail has been detected. SF works in the reverse way. Optional pull-up resistors will be functional if DEL ERROR SCAN EXTERNAL PULL-UP SOURCE, Terminal R, is connected to an external voltage source.

CIRCUIT THEORY

Data Shifting and Interface

The right-hand side of Figure 6 shows the data-shift, latch, and interface circuits common to both control and expander cards. Serial data enters through the DATA IN or EX DATA IN, Terminals W and L, and are shifted through the serially connected shift registers, IC4, IC9, and IC14. The clock signal is developed at Pins 1 and 9 of these IC's. A power-initialization reset signal is developed at Pins 6 and 14. Once the data have been shifted into the registers and validated, they are then loaded into the data latches, IC5, IC10, and IC15, through the LOAD CMND pulse to Pin 9. These latched data will then drive common-emitter, NPN Darlington Pairs, QZ1, QZ2, and QZ3.

For serially connected decoders, the serial data are shifted to an adjacent card from Pin 2 of IC4, through the MULTIWORD DATA OUTPUT, Terminal D. Data are also shifted through Pin 2 of flip-flop IC2, of the last card in a series of connected decoder cards, to DOUBLESCAN DATA OUTPUT, Terminal E, for hardwire connection to the control decoder's DOUBLESCAN DATA INPUT, Terminal M. Inputs to Terminal M are the source for data in doublescan procedures.

The data latches will hold the previously accepted valid data while the shift registers are shifting through the next encoder message, and processing the received data. The registers may be reset by an error-scan signal from Pin 12 of IC3, or by a manual low at $\overline{\text{REG RESET}}$, Terminal 19.

Circuit Control and Data-Shift Clocking

Toggling of Pin 1 of flip-flop IC1A initiates the decoding sequence. This toggling can be initiated by an end-of-message signal from the WORD jumper associated with IC16, by an abort signal from IC13A-9, or by the power-initialization circuit through IC17E-12.

When IC1A is toggled at its Q output, the delay network, R7-C3, will cause a pulse from IC6B-6. This pulse, gated through IC11C-10, will cause the various counters to be reset in a manner similar to power initialization. This procedure causes a high to be developed at Pin 2 of the subword counter, IC20. The baud-rate counter, IC24, is now free, enabled by IC18A-3, to generate a clock pulse, proportional to the baud rate, at Pin 1 of IC23. These clock pulses are then counted by the bit counter, IC23, which then generates the binary code corresponding to the bit pattern for each subword and generates the clock pulse for data-bit shifting of the data through the shift registers, IC4, IC9, and IC14.

Each shifting of eight bits causes the subword counter, IC20, to be incremented. The fifth subword causes a clock output to Input Pin 13 of the word counter, IC16.

The very first subword corresponds to the message header and a high will be developed during this time at IC20-2. This high, through IC21A and IC18B-4, will prevent data from being shifted into the shift registers during the existence of the header. Also, during the presence of the header, IC9A will generate a counter-reset pulse when a high (header generates a continuous low) is detected. This reset signal will continuously reset the control counters unless at least eight full low bits of a true header have been received by the decoder. As this event occurs, the subword counter will have incremented and IC20-1 will go high.

That signal will then enable the output of Pin 10 of IC6C to generate a momentary high when the mark-to-space transition is detected at IC6C-11. This transition signals the beginning of the data message. The decoder-control circuit will now be free to shift the incoming data by utilizing the clock pulse from IC18B-4, as generated through the baud and bit counters and the oscillator clock pulse, through Pin 3 of IC18A.

Received-Data Qualification

As the data are shifted through the shift registers, the flip-flop pair, IC19A and IC19B, will generate the parity information from the input serial data. This is accomplished by selectively clocking the flip-flop combination, Pins 3

and 11, when a low appears, at the first output, at Pin 5, of the initial shift register, IC14. The parity-totalizer flip-flop combination is maintained in reset during the code's header phase through a high on IC17C-6. The clocking to the combination is disabled during the time that the last two bits of each word are shifted into the shift registers by outputs at the bit counter at Pins 5 and 6 of IC23, and during the fourth subword, as indicated by a high at Pins 7 and 10 of the subword counter, IC20. Thus, the parity flip-flop combination will totalize the data bits, but it will not include the information from the two incoming parity bits. At the completion of a word shift, the incoming parity-bit data will be compared against the generated parity data at IC7A-3 and IC7C-10. If the generated parity bits from IC19A and IC19B do not compare with the transmitted bits, an abort signal is gated through IC12A-9.

This high, through Pin 9 of IC13A, will cause the initiate flip-flop, Pin 2 of IC1A, to be toggled. This procedure is performed for singlescan and for the first half of a doublescan message.

For singlescan applications, the message length equals the actual number of data words required. The subword and word counters, IC20 and IC16, respectively, generate output signals equivalent to the number of words required. If the data are received validly, the WORD jumper will deliver a LOAD CMND signal when the number of words received begins to exceed the designated word count. This signal will cause the output-data latches, IC5, IC10, and IC15, to be updated. The decoder will also be reinitialized, by toggling Pin 2 of IC1A, when the output from the BAUD jumper is gated through IC18C along with the WORD jumper output.

For doublescan operation, the normal singlescan message is transmitted twice, in the same order as if it were single-scanned. For the second pass, the output data are serially channeled back through DOUBLE SCAN DATA INPUT, Terminal M. The input serial data are inverted, before being serially shifted through the shift registers, by Pin 11 of IC7D.

The SCAN jumper selects an output from either the subword or the word counter corresponding to the first half of a full-word message. This output toggles the double-scan flip-flop, IC1B-12, to indicate the start of the second pass of the message words. The data from the first pass are compared against the incoming data at IC7B-4. This output is gated with the output from the doublescan flip-flop, IC1B-12, and a signal window from counters IC20 and IC23, corresponding to a pulse signal occurring after the data have been shifted and before the bit address is incremented. This comparison is made for each shifted bit, but not for the header. The header transmission is signalled by a low at Pin 13 of IC12C. If the comparison fails during the second scan, an output from Pin 9 of IC13A will cause the initiate flip-flop to be toggled through IC11B-3.

If no abort condition is created, eventually the word jumper will deliver a signal which will latch the serially shifted data into the output-storage registers, IC5, IC10, and IC15, through Pin 1 of each. This same signal, gated with the BAUD jumper output, will cause the initiate flip-flop, Pin 2 of IC1A, to be toggled. This will initiate a new decoding sequence.

Scan Failure

Under normal scan procedure, the scan-fail counter, IC3, is being periodically reset at Pin 11 by the register-load-command signal. If load command should cease, this counter will accumulate the clock pulses from the precisely timed output from Pin 3 of IC24. If a load signal does not occur before the counter reaches its predetermined output, approximately 5 to 10 seconds after reset, then Pin 15 of IC3 will deliver a high which will disable the input clock. This high will then remain until a valid load-command signal resets the baud counter. This high will also initiate the SCAN FAIL indicator. If the output-register-reset option is used, these registers will be reset when the scan fail begins. For added single-scan security, Q1 monitors the presence of the 1 and 0 check bits in the data code, and it disables the output register's load command when these check bits are not present at the register outputs, Pins 11 and 2 of IC14.

Release Data

Output-register-load command also sets the flip-flop, Pin 12 of IC2B. This flip-flop drives the RELEASE DATA lamp until the flip-flop is reset by the bit counter, IC23.

Metallic-Line Driver, Option HB-44985

In the normal communication mode, the line driver, at the sending end, will cause a current to flow into either the HI or the LO input line, Figure 7. With valid data, the HI line will be high when the data output is high, and the LO line will be high when the data output is low. In either case, the output of either IC1 or IC2 will be in conduction.

When the transistor in IC1 is conducting, IC1-6 and -8 will be low, IC3A-3 will be high and DECODER DATA INPUT, Terminal DI, will be high. IC3A and IC3B form an R-S flip-flop for latching the input signal.

When the transistor in IC2 is conducting, IC2-6 and -8 are low, and this low is propagated through the R-S flip-flop to Terminal DI.

So long as normal signals are received, the outputs of IC1 and IC2 will always be of opposite polarity, and they will thereby hold IC3C-10 high. This passes through IC3D, IC4D, and IC4C where this signal appears as a low at IC4C-10. The resulting high at IC4B-4 indicates, at DECODER CD INPUT, Terminal $\overline{CF}$, that carrier is present.

Similarly, the low at IC4C-10 holds IC4A-3 high, causes DS1, LINE CURRENT, to glow, and holds Q1 in a conducting state so that LINE-CURRENT-FAILURE DETECTION OUTPUT, Terminal SD, is held low.

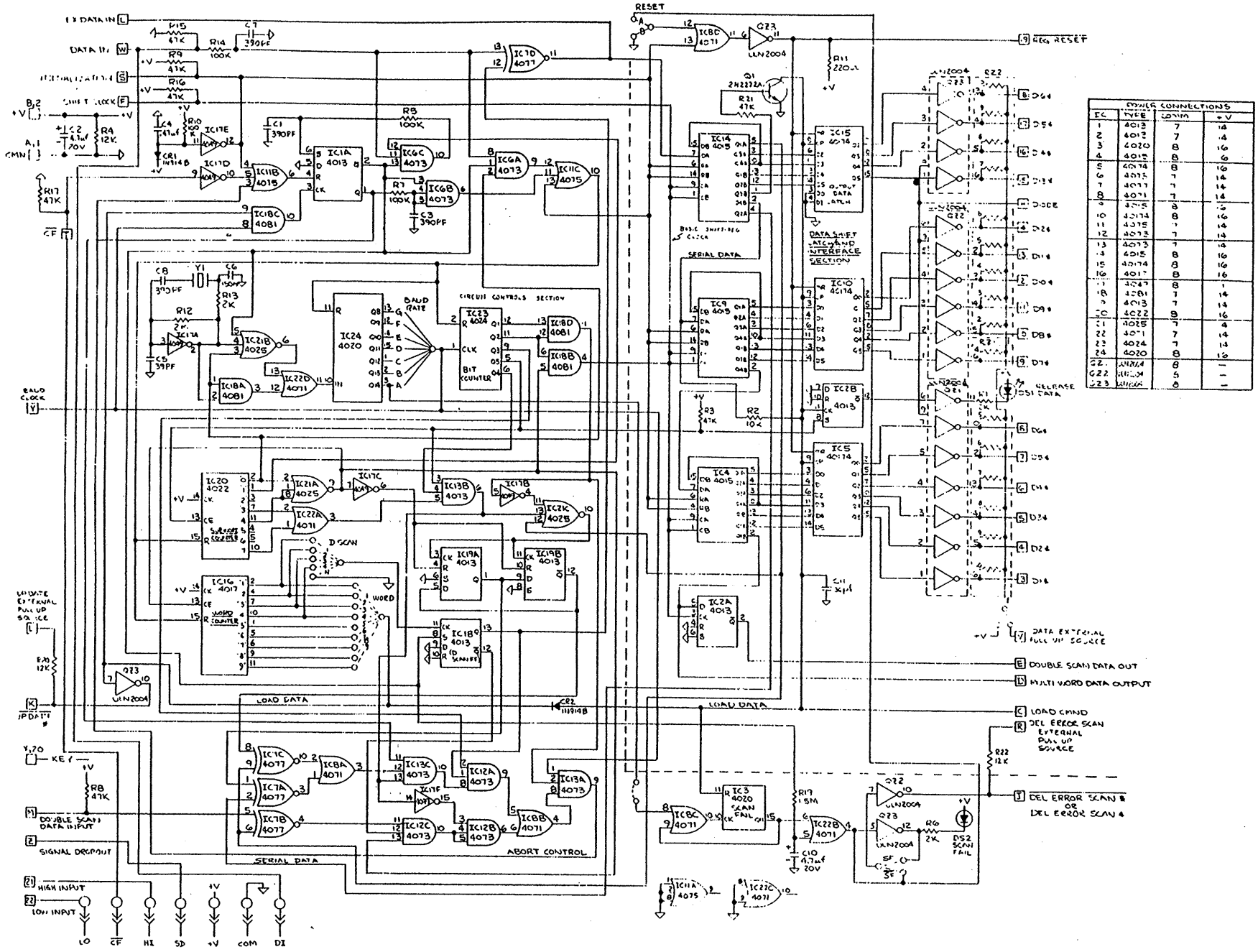
To indicate a change of state, the transmitter raises both HI and LO input lines to a logic high. In response, the outputs of both IC1 and IC2 become high simultaneously. The two highs at the input of IC3C drive its output, IC3C-10, low. This low appears as a high at IC4C-10, and CF goes low to indicate loss of signal. At the same time, IC4A-3 will go low, DS1 will extinguish, and Q1 will become non-conducting so that Terminal SD will go high. The simultaneous high outputs from the two optoisolators will cause the R-S flip-flop to place a high at Terminal DI.

It may be noted that if both input lines were to go low simultaneously the same change-of-state response described in the foregoing would occur.

PARTS LIST

CIRCUIT SYMBOL	DESCRIPTION	PART NUMBER
	Model 66A DEC Decoder Controller, Assembly HB-44960	
C1, 3, 7, 8	Capacitor, dipped mica, 390pF, 5%, 100V, Electromotive DM-10, or eq.	H-1080-379
C2, 10	Capacitor, tantalum, 4.7μF, 20%, 20V, Kemet T324B475M020AS, or eq.	H-1007-711
C4	Capacitor, ceramic, 0.47μF, +80 −20%, 50V, Sprague 5C023474D8500C5, or eq.	H-1007-939
C5	Capacitor, dipped mica, 39pF, 5%, 100V, Electromotive DM-10, or eq.	H-1080-385
C6	Capacitor, dipped mica, 150pF, 5%, 100V, Electromotive DM-10, or eq.	H-1080-386
C9, 10	Not used	
C11	Capacitor, dipped mica, 36pF, 5%, 500V, Electromotive DM-15, or eq.	HA-16512
CR1, 2	Diode, silicon, Type 1N914B/1N4448	HA-26482
DS1, 2	Lamp, LED, Dialight 550-0102, or eq.	HA-39568
IC1, 2, 19	Dual D-type flip-flop; RCA CD4013AE, or eq.	H-0615-1
IC3, 24	Fourteen-stage binary counter, Fairchild F4020PC only	H-0615-73
IC4, 9, 14	Dual, 4-stageshift register, RCA CD4015AE, or eq.	H-0615-25
IC5, 10, 15	Hex D-type flip-flop, Fairchild F40174PC, or eq.	H-0615-70
IC6, 12, 13	Triple, 3-input AND gate, RCA CD4073BE, or eq.	H-0615-32
IC7	Quad, EXCL-NOR gate, Motorola MC14077BP, or eq.	H-0615-71
IC8, 22	Quad, 2-input OR gate, RCA CD4071BE, or eq.	H-0615-24
IC11	Triple, 3-input OR gate, RCA CD4075BE, or eq.	H-0615-33
IC16	Decade counter/divider, RCA CD4071AE, or eq.	H-0615-38
IC20	Divide-by-8 counter, divider, RCA CD4022AE, or eq.	H-0615-6
IC17	Hex inverting buffer, Fairchild F4049PC only	H-0615-61
IC18	Quad, 2-input AND gate, RCA CD4081BE, or eq.	H-0615-31
IC21	Triple, 3-input NOR gate, RCA CD4025AE, or eq.	H-0615-20
IC23	Seven-stage binary counter, RCA CD4024AE, or eq.	H-0615-14
Q1	Transistor, silicon, NPN, Type 2N2222A	HA-37445
QZ1, 2, 3	Transistor array, TI ULN2004AN, or eq.	H-0720-1
R1 - 22	Resistor, fixed, composition, 5%, 1/4W, value on schematic, Allen Bradley CB, or eq.	H-1009-(xxx)
R11	Not used	
RZ1, 2	Optional resistor network, 12K, 2%, 2.7 w/pkg., Beckman 898-3	HA-45440
Y1	Piezoelectric crystal, frequency as specified	HA-37440-(xx)
—	Bar, shorting, single	HA-42904
—	Schematic (Figure 6)	HE-44964

CIRCUIT SYMBOL	DESCRIPTION	PART NUMBER
	Model 66A DEC EXP Decoder Expander, Assembly HB-44965	
C1	Not used	
C2	Capacitor, tantalum, 4.7μF, 20%, 20V, Kemet T324B475M020AS, or eq.	H-1007-711
IC1	Not used	
IC2	Dual D-type flip-flop, RCA CD4013, or eq.	H-0615-1
IC3	Not used	
IC4, 9, 14	Dual, 4-stage shift register, RCA CD4015AE, or eq.	H-0615-25
IC5, 10, 15	Hex D-type flip-flop, Fairchild F40174PC, or eq.	H-0615-70
IC6, 7, 8, 11, 12, 13	Not used	
QZ1, 2, 3	Transistor array, TI ULN2004AN, or eq.	H-0720-1
R1, 5-10	Not used	
R2, 3, 4, 11	Resistor, fixed, composition, 5%, 1/4W, value on schematic, Allen Bradley CB, or eq.	H-1009-(xxx)
	Metallic-Line Receiver, Option HB-44985	
C1	Capacitor, tantalum, 1μF, 20%, 35V, Kemet T324B105M035AS, or eq.	H-1007-496
C2	Capacitor, metallized polyester, 0.22μF, 10%, 250V, Seacor 106-0.1, or eq.	H-1007-1255
CR1	Varistor, 15.2-16.8V breakdown, Gen. Semiconductor 1.5KE16CA	HA-44982
CR2, 3	Diode, surmetic, Type 1N4001	HA-38876
DS1	Lamp, LED, Dialight 550-0102, or eq.	HA-39568
IC1, 2	Optical isolator, Hewlett-Packard 5082-4371, or eq.	HA-29592
IC3, 4	Quad, 2-input NAND gate, RCA CD4011AE, or eq.	H-0615-5
Q1	Transistor, silicon, NPN Type 2N2222A	HA-37445
R1-9	Resistor, fixed, composition, 5%, 1/4W, value on schematic, Allen Bradley CB, or eq.	H-1009-(xxx)
RT1	Thermistor, 47 ohms, 20%, 125V, Murata PTH61AR470M2B151, or eq.	HA-41942
—	Schematic (Figure 7)	HC-44989



POWER CONNECTIONS			
IC	TYPE	COMM	+V
1	4013	7	14
2	4012	7	14
3	4020	8	16
4	4015	8	16
5	4014	8	16
6	4015	8	16
7	4077	7	14
8	4071	7	14
9	4015	8	16
10	4014	8	16
11	4015	8	16
12	4013	7	14
13	4073	7	14
14	4015	8	16
15	4014	8	16
16	4017	8	16
17	4049	8	-
18	4081	7	14
19	4013	7	14
20	4022	8	16
21	4025	7	14
22	4071	7	14
23	4024	7	14
24	4020	8	16
Q22	ULN2004	8	-
Q22	ULN2004	5	-
Q23	ULN2004	8	-

Figure 6. Schematic of circuit, Model 66A DEC and 66A DEC EXP.

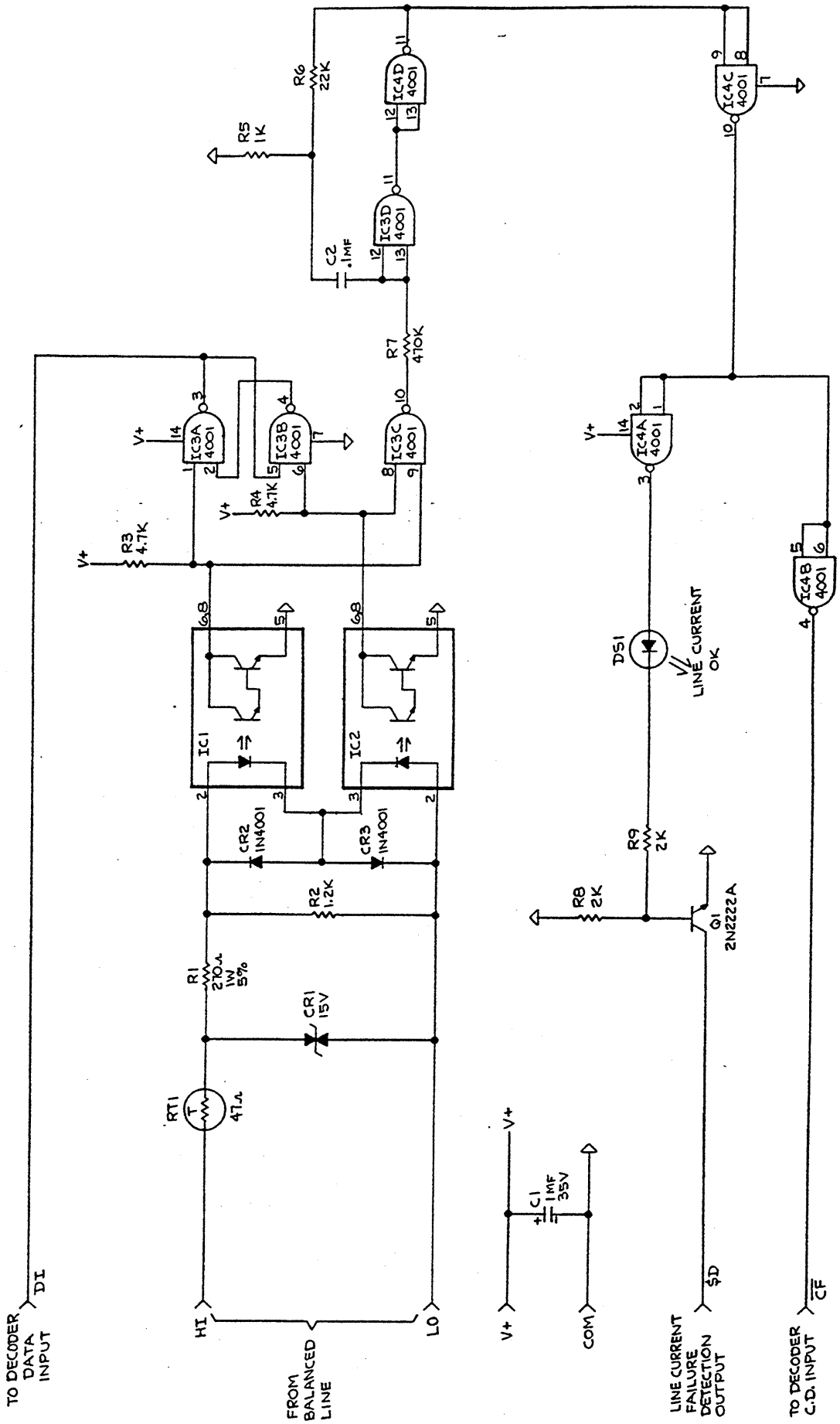


Figure 7. Schematic of circuit for Metallic-Line Receiver, Option HB-44985.